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IN THE CLAIMS

Please cancel claims 5, 8-9 and 12-13 without prejudice.

Please amend claims 1-2, 6-7 and 10 as follows:

1. (currently amended) A system for addressing a data storage unit used in at least one of server and client computers, which comprises:

means for converting a format of data on an external bus such that the data are accessed on an internal bus for use in the system;

a memory card module connected to the internal bus for storing data [~~on~~] transmitted through the internal bus, wherein the memory card module includes a plurality of memory modules each having a plurality of equally-sized memory blocks, each memory block being divided into a predetermined number of equally-sized sub-memories such that the memory module has a hierarchical memory configuration, wherein the memory card module includes a PCI-to-memory controller, which is disposed between the internal bus and the memory module as a bridge, for controlling access to the plurality of sub-memories, and

wherein the PCI-to-memory controller includes:

a PCI interface controlling unit for performing a standard PCI command, control and data signal processing, the PCI interface controlling unit including a register block having a lower address bit, an upper address bit and a select bit, wherein the lower address bit represents addresses included in the range of an address region within a memory map, the upper address represents an address set to be used when a memory address region is beyond the address region of the memory map, and the select bit is used to directly access the memory module; and

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a plurality of memory controlling units for performing a direct read/write operation for the sub-memories in response to the PCI command from the PCI interface controlling unit; and

means for writing data on the internal bus to the memory module and reading out the data therefrom.

2. (currently amended) The system of claim 1, wherein the internal bus is a PCI (Peripheral Component Interconnect Bus) interface bus.

3. (previously presented) The system of claim 1, wherein the external bus is a SCSI (Small Computer System Interface) bus.

4. (previously presented) The system of claim 1, wherein the memory card module is composed of any one of SDRAM(Synchronous Dynamic Random Access Memory), rambus DRAM(Dynamic Random Access Memory), DDR(Double Data Rate) or other equivalent memories.

5. (canceled)

6. (currently amended) The system of claim [~~5~~] 1, wherein the predetermined number is four.

7. (currently amended) The system of claim [~~5~~] 1, wherein signals inputted to the memory card module of the hierarchical memory configuration are compensated again at memory module and memory block stages.

8-9. (canceled)

10. (currently amended) The system of claim [~~8~~] 1, wherein the PCI-to-memory controller activates any of the plurality of sub-memories to be actually accessed and maintains the remaining in a low power mode.

11-13. (canceled)